NUD3112

Integrated Relay, Inductive Load Driver

This device is used to switch inductive loads such as relays, solenoids incandescent lamps, and small DC motors without the need of a free−wheeling diode. The device integrates all necessary items such as the MOSFET switch, ESD protection, and Zener clamps. It accepts logic level inputs thus allowing it to be driven by a large variety of devices including logic gates, inverters, and microcontrollers.

Features

- Provides a Robust Driver Interface Between D.C. Relay Coil and Sensitive Logic Circuits
- Optimized to Switch Relays of 12 V Rail
- Capable of Driving Relay Coils Rated up to 6.0 W at 12 V
- Internal Zener Eliminates the Need of Free−Wheeling Diode
- Internal Zener Clamp Routes Induced Current to Ground for Quieter Systems Operation
- Low $V_{DS(ON)}$ Reduces System Current Drain
- Pb−Free Packages are Available

Typical Applications

- Telecom: Line Cards, Modems, Answering Machines, FAX
- Computers and Office: Photocopiers, Printers, Desktop Computers
- Consumer: TVs and VCRs, Stereo Receivers, CD Players, Cassette Recorders
- Industrial: Small Appliances, Security Systems, Automated Test Equipment, Garage Door Openers

ON Semiconductor®

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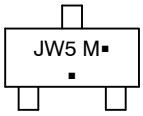
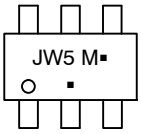
MARKING DIAGRAMS

SOT−23
CASE 318
STYLE 21



JW5 = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

SC−74
CASE 318F
STYLE 7



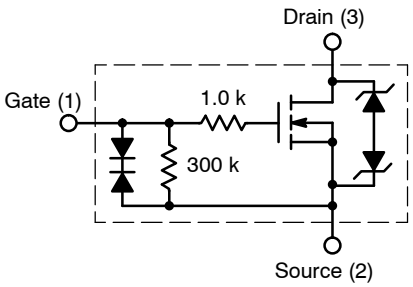
JW5 = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

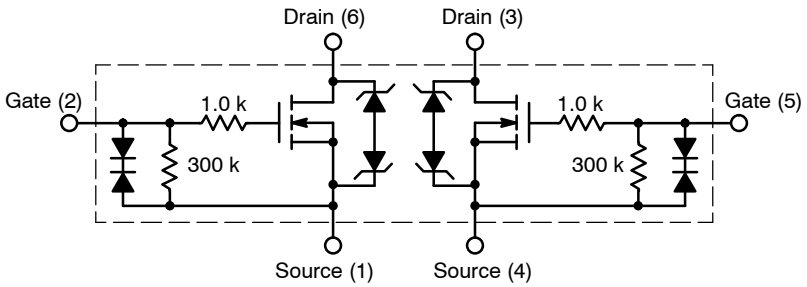
Device	Package	Shipping†
NUD3112LT1	SOT−23	3000/Tape & Reel
NUD3112LT1G	SOT−23 (Pb−Free)	3000/Tape & Reel
NUD3112DMT1	SC−74	3000/Tape & Reel
NUD3112DMT1G	SC−74 (Pb−Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

INTERNAL CIRCUIT DIAGRAMS



CASE 318



CASE 318F

MAXIMUM RATINGS (T_J = 25°C unless otherwise specified)

Symbol	Rating		Value	Unit
V_{DSS}	Drain to Source Voltage – Continuous		14	V_{dc}
V_{GS}	Gate to Source Voltage – Continuous		6	V_{dc}
I_D	Drain Current – Continuous		500	mA
E_z	Single Pulse Drain–to–Source Avalanche Energy ($T_{Jinitial}$ = 25°C)		50	mJ
T_J	Junction Temperature		150	°C
T_A	Operating Ambient Temperature		–40 to 85	°C
T_{stg}	Storage Temperature Range		–65 to +150	°C
P_D	Total Power Dissipation (Note 1) Derating Above 25°C	SOT–23	225 1.8	mW mW/°C
P_D	Total Power Dissipation (Note 1) Derating Above 25°C	SC–74	380 3.0	mW mW/°C
$R_{\theta JA}$	Thermal Resistance Junction–to–Ambient (Note 1)	SOT–23 SC–74	556 329	°C/W
ESD	Human Body Model (HBM) According to EIA/JESD22/A114		2000	V

1. Mounted onto minimum pad board.

TYPICAL ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Characteristic	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
V_{BRDSS}	Drain to Source Sustaining Voltage (Internally Clamped) (I_D = 10 mA)	14	16	17	V
B_{VGSO}	I_g = 1.0 mA	–	–	8	V
I_{DSS}	Drain to Source Leakage Current (V_{DS} = 12 V , V_{GS} = 0 V, T_A = 25°C) (V_{DS} = 12 V, V_{GS} = 0 V, T_A = 85°C)	– –	– –	20 40	μA
I_{GSS}	Gate Body Leakage Current (V_{GS} = 3.0 V, V_{DS} = 0 V) (V_{GS} = 5.0 V, V_{DS} = 0 V)	– –	– –	35 65	μA
ON CHARACTERISTICS					
$V_{GS(th)}$	Gate Threshold Voltage (V_{GS} = V_{DS}, I_D = 1.0 mA) (V_{GS} = V_{DS}, I_D = 1.0 mA, T_A = 85°C)	0.8 0.8	1.2 –	1.4 1.4	V
$R_{DS(on)}$	Drain to Source On–Resistance (I_D = 250 mA, V_{GS} = 3.0 V) (I_D = 500 mA, V_{GS} = 3.0 V) (I_D = 500 mA, V_{GS} = 5.0 V) (I_D = 500 mA, V_{GS} = 3.0 V, T_A=85°C) (I_D = 500 mA, V_{GS} = 5.0 V, T_A=85°C)	– – – – –	– – – – –	1.2 1.3 0.9 1.3 0.9	Ω
$I_{DS(on)}$	Output Continuous Current (V_{DS} = 0.25 V, V_{GS} = 3.0 V) (V_{DS} = 0.25 V, V_{GS} = 3.0 V, T_A = 85°C)	300 200	400 –	– –	mA
g_{FS}	Forward Transconductance (V_{OUT} = 12.0 V, I_{OUT} = 0.25 A)	350	490	–	mmhos

TYPICAL ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Characteristic	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS					
C_{iss}	Input Capacitance (V_{DS} = 12 V, V_{GS} = 0 V, f = 10 kHz)	–	23	–	pF
C_{oss}	Output Capacitance (V_{DS} = 12 V, V_{GS} = 0 V, f = 10 kHz)	–	30	–	pF
C_{rss}	Transfer Capacitance (V_{DS} = 12.0 V, V_{GS} = 0 V, f = 10 kHz)	–	7	–	pF

SWITCHING CHARACTERISTICS

Symbol	Characteristic	Min	Typ	Max	Units
	Propagation Delay Times:				nS
t_{PHL}	High to Low Propagation Delay; Figure 1 (V_{DS} = 12 V, V_{GS} = 5.0 V)	–	21	–	
t_{PLH}	Low to High Propagation Delay; Figure 1 (V_{DS} = 12 V, V_{GS} = 5.0 V)	–	91	–	
	Transition Times:				nS
t_f	Fall Time; Figure 1 (V_{DS} = 12 V, V_{GS} = 5.0 V)	–	36	–	
t_r	Rise Time; Figure 1 (V_{DS} = 12 V, V_{GS} = 5.0 V)	–	61	–	

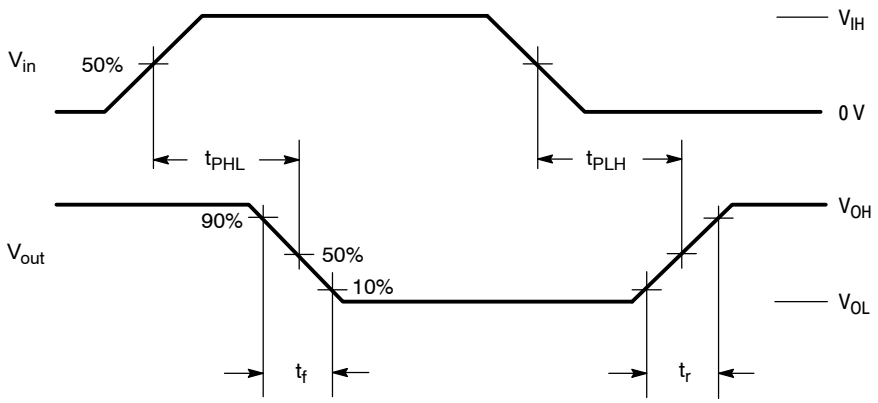


Figure 1. Switching Waveforms

TYPICAL PERFORMANCE CURVES (T_J = 25°C unless otherwise specified)

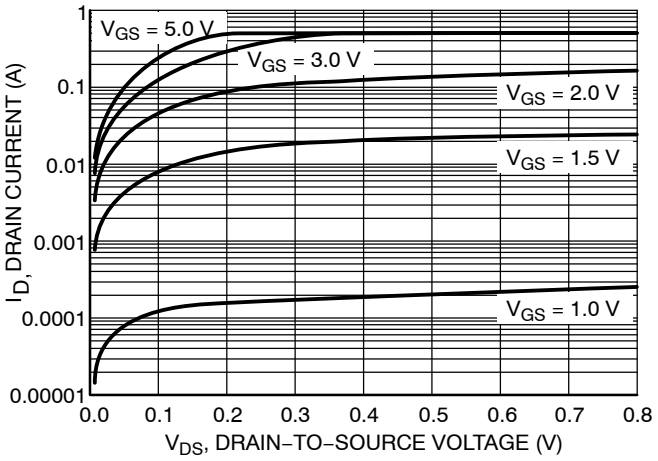


Figure 2. Output Characteristics

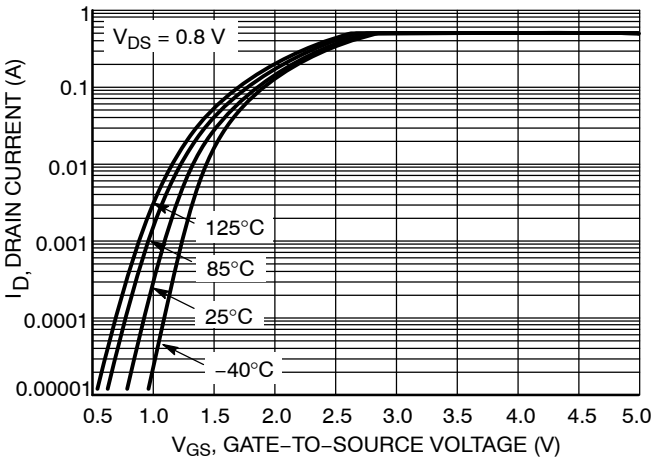


Figure 3. Transfer Function

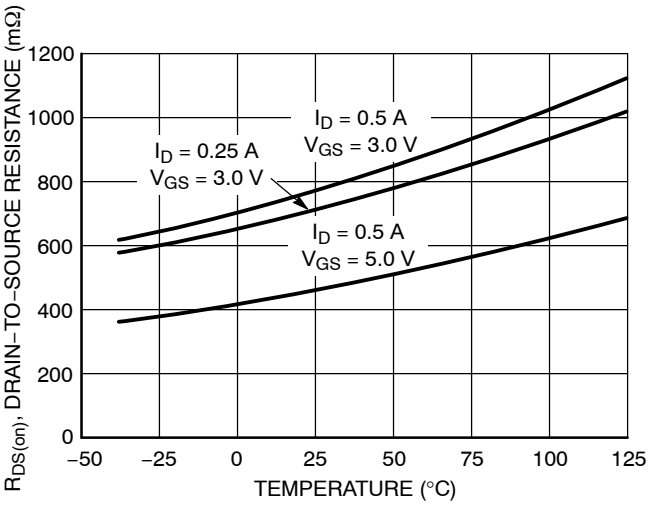


Figure 4. On−Resistance Variation vs. Temperature

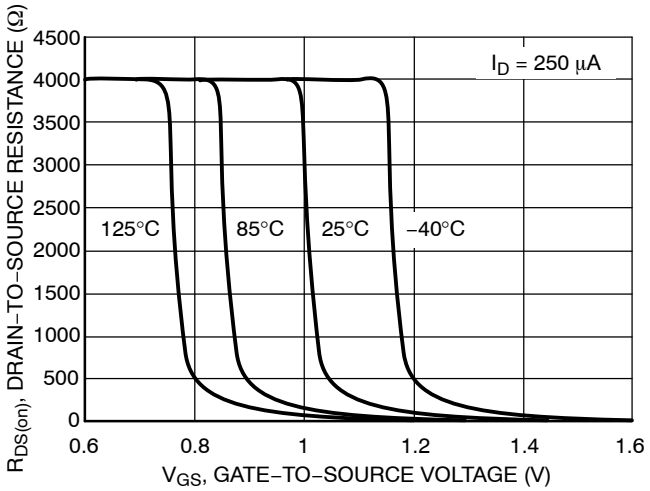


Figure 5. $R_{DS(ON)}$ Variation vs. Gate−to−Source Voltage

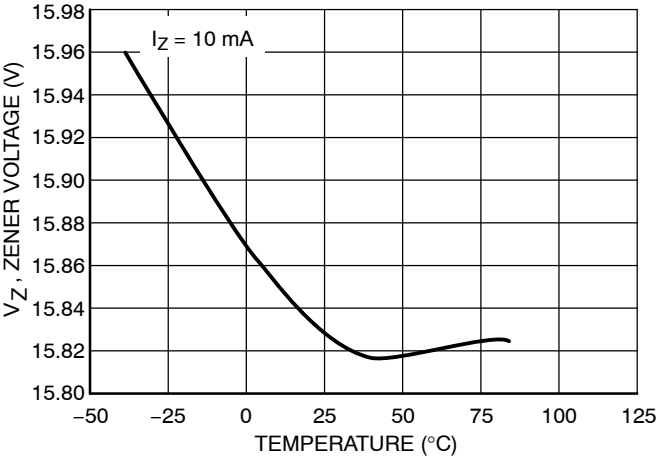


Figure 6. Zener Voltage vs. Temperature

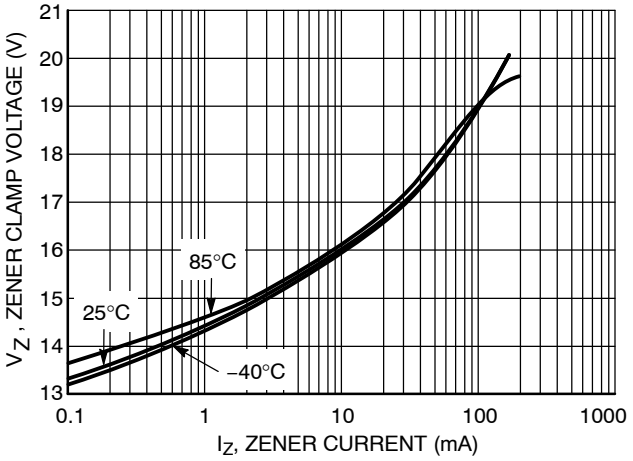


Figure 7. Zener Clamp Voltage vs. Zener Current

TYPICAL PERFORMANCE CURVES (T_J = 25°C unless otherwise specified)

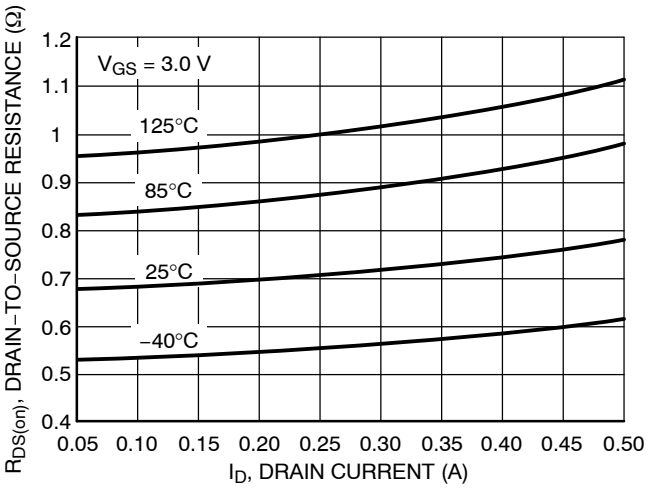


Figure 8. On−Resistance vs. Drain Current and Temperature

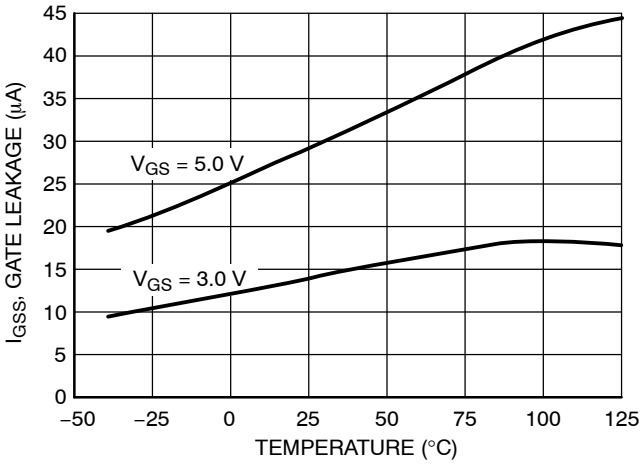


Figure 9. Gate Leakage vs. Temperature

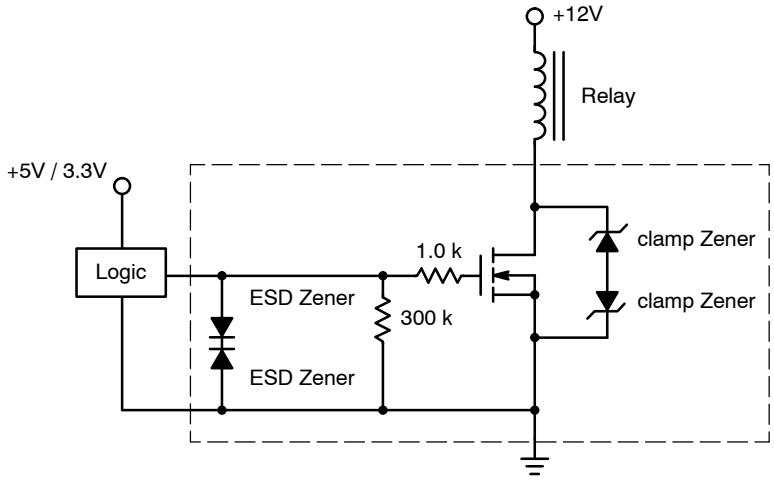
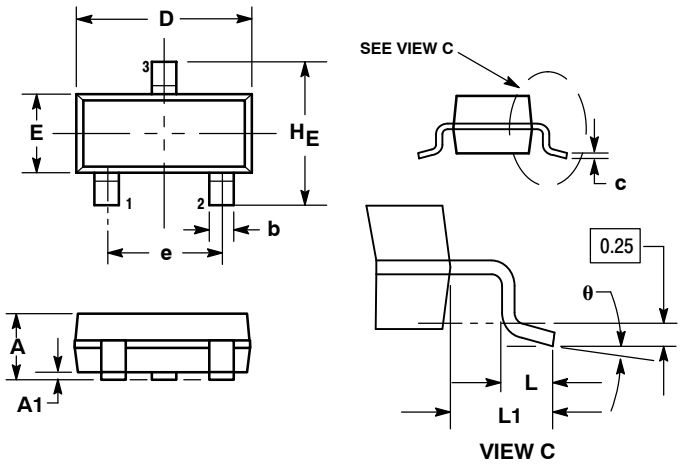


Figure 10. Typical Application Circuit

PACKAGE DIMENSIONS

SOT−23 (TO−236)
CASE 318−08
ISSUE AN

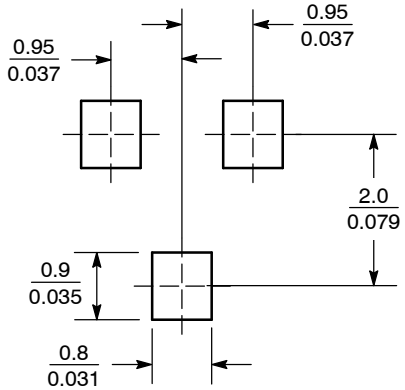


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 318−01 THRU −07 AND −09 OBSOLETE, NEW STANDARD 318−08.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1.00	1.11	0.035	0.040	0.044
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.37	0.44	0.50	0.015	0.018	0.020
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.081
L	0.10	0.20	0.30	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
H_E	2.10	2.40	2.64	0.083	0.094	0.104

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

SOLDERING FOOTPRINT*

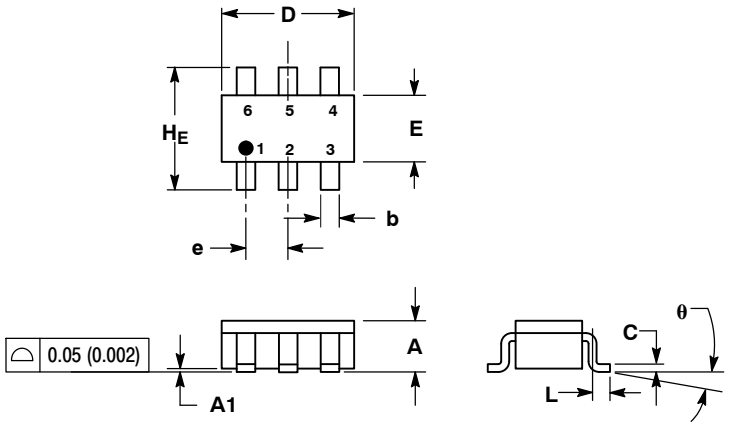


SCALE 10:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

SC−74
CASE 318F−05
ISSUE M

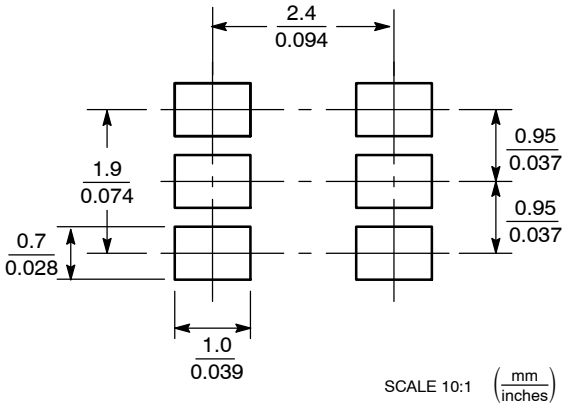


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 318F−01, −02, −03, −04 OBSOLETE. NEW STANDARD 318F−05.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.90	1.00	1.10	0.035	0.039	0.043
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.25	0.37	0.50	0.010	0.015	0.020
c	0.10	0.18	0.26	0.004	0.007	0.010
D	2.90	3.00	3.10	0.114	0.118	0.122
E	1.30	1.50	1.70	0.051	0.059	0.067
e	0.85	0.95	1.05	0.034	0.037	0.041
L	0.20	0.40	0.60	0.008	0.016	0.024
H_E	2.50	2.75	3.00	0.099	0.108	0.118
θ	0°	–	10°	0°	–	10°

STYLE 7:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

SOLDERING FOOTPRINT*



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